CPU Unit Descriptions

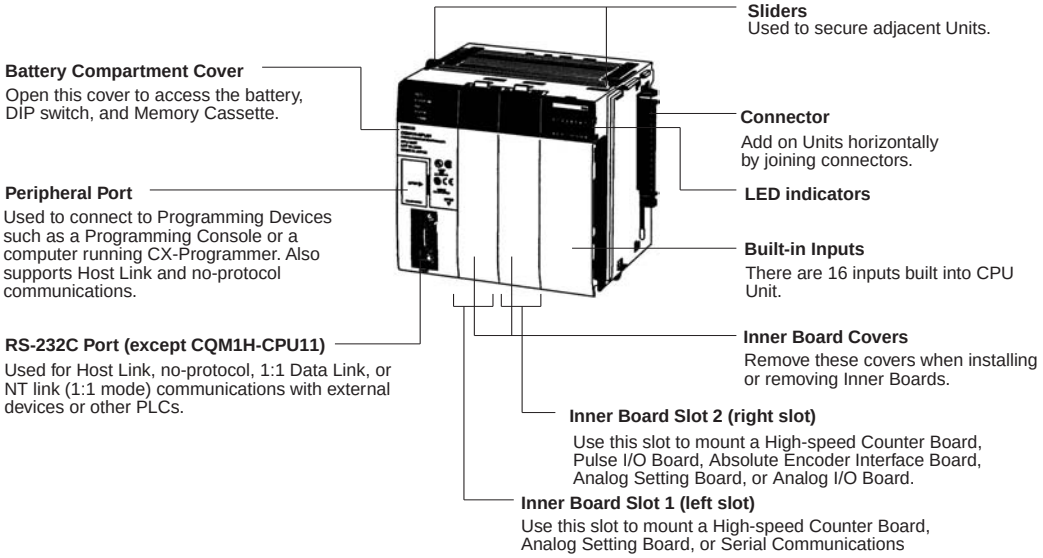
CQM1H CPU Units
CQM1H-CPU□□

CPU Units

The four models of CPU Units can be broadly divided into two groups: Models that support Inner Boards and the Controller Link Unit, and models that do not. The CPU Units also vary in their program capacities, I/O capacities, memory capacities, and the presence of an RS-232C port, as shown in the *Basic Specifications* table, below.

■ CPU Unit Overview

The following illustration shows the main components of a CQM1H-CPU61 CPU Unit.



■ Basic Specifications

Model	I/O capacity (See note.)	Program capacity (words)	DM capacity (words)	EM capacity (words)	CPU Unit built-in inputs	Built-in serial ports		Inner Boards	Controller Link Unit
						Peripheral port	RS-232C port		
CQM1H-CPU61	512	15.2 K	6 K	6 K	DC: 16	Yes	Yes	Supported	
CQM1H-CPU51		7.2 K	6 K	None					
CQM1H-CPU21	256	3.2 K	3 K					Not supported	
CQM1H-CPU11							No		

Note: I/O capacity = Number of input points (≤ 256) + Number of output points (≤ 256).

■ Maximum Number of Units

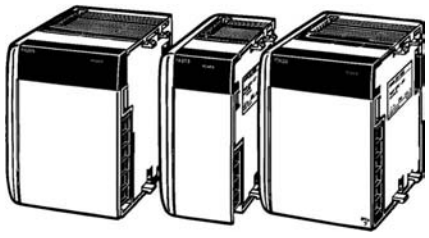
CPU Unit	Controller Link Unit	Inner Boards	I/O Units and Dedicated I/O Units
CQM1H-CPU61	1 max.	2 max.	11 max. (total)
CQM1H-CPU51			
CQM1H-CPU21	Not supported.	Not supported.	
CQM1H-CPU11			

Power Supply Units and I/O Expansion Units

■ Power Supply Units

Both AC and DC Power Supply Units are available. The AC Power Supply Units require a power supply input from 100 to 240 V AC and two of the AC Power Supply Units are equipped with a 24-V DC power supply output.

The CQM1H's left End Cover is part of the Power Supply Unit.



CQM1-PA206 CQM1-PA203 CQM1-PD026
CQM1-PA216

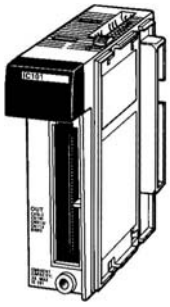
Specifications

Name	Model number	Specifications			
		Supply voltage	Operating voltage range	Output capacity	Service power supply
AC Power Supply Units	CQM1-PA203	100 to 240 V AC, 50/60 Hz (wide range)	85 to 265 V AC	5 V DC: 3.6 A (18 W)	None
	CQM1-PA206			5 V DC: 6 A 24 V DC: 0.5 A (30 W total, see note)	24 V DC: 0.5 A
	CQM1-PA216	100 or 230 V AC (selectable), 50/60 Hz		5 V DC: 6 A 24 V DC: 0.5 A (30 W total, see note)	
DC Power Supply Units	CQM1-PD026	24 V DC	20 to 28 V DC	30 W 5 V DC: 6 A	None

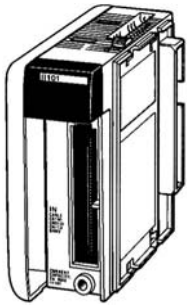
Note: The total power consumed at 5 V DC and 24 V DC must be less than 30 W.
$(5 \times \text{Current consumed at 5 V DC}) + (24 \times \text{Current consumed at 24 V DC}) \leq 30$ W

■ I/O Expansion Units

Use Expansion I/O Blocks to split the configuration into more than one group, allowing greater flexibility with mounting space as well as the use of at least 12 I/O Units or Dedicated I/O Units. Expansion Units can be used with any CQM1H CPU Unit.



CQM1H-IC101



CQM1H-II101

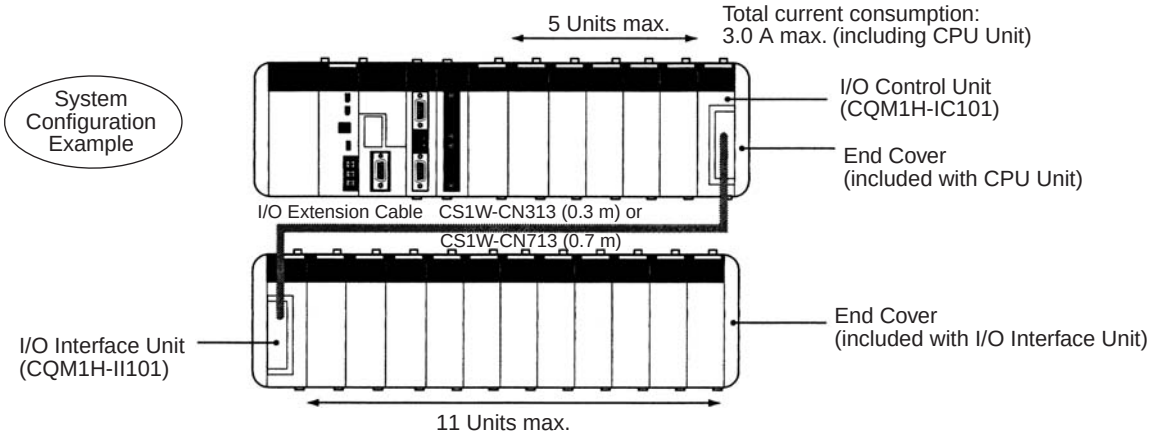
Maximum Number of Units Mountable

CPU Unit model	CPU Block only	CPU Block + I/O Expansion Block			
	CPU Block	CPU Block			I/O Expansion Block
	I/O Units + Dedicated I/O Units	Controller Link Unit	Inner Boards	I/O Units + Dedicated I/O Units	I/O Units + Dedicated I/O Units
CQM1H-CPU61	11 Units max. (see note 1)	1 Unit	2 Boards max.	5 Units max. (see note 2)	11 Units max. (see note 3)
CQM1H-CPU51					
CQM1H-CPU21		Not supported	Not supported		
CQM1H-CPU11					

Note: 1. Ensure that the total current consumption of the mounted Units (CPU Unit, Controller Link Unit, Inner Boards, I/O Units, and Dedicated I/O Units)

2. Ensure that the total current consumption of the mounted Units (CPU Unit, Controller Link Unit, Inner Boards, I/O Units, Dedicated I/O Units, and I/O Control Units) does not exceed 3.0 A.

3. Ensure that the total current consumption of the mounted Units (I/O Interface Units, I/O Units, and Dedicated I/O Units) does not exceed 2.0 A.



Total current consumption: 2.0 A max. (I/O Units and Dedicated I/O Units)

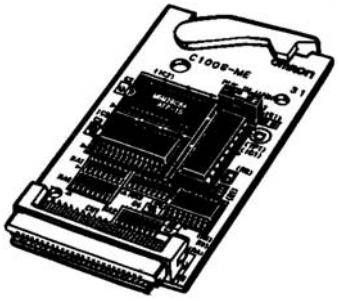
Memory Cassettes

An optional Memory Cassette can be used to store the user program, PLC Setup, and other data in ROM so that vital data will not be lost in the event of battery expiration or careless programming/monitoring operations.

If the PLC's settings need to be changed to execute another process, the entire software setup and user program can be changed just by exchanging the Memory Cassette and rebooting the PLC.

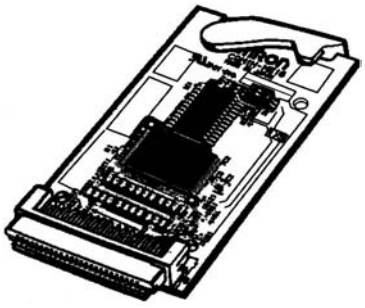
EEPROM:

CQM1-ME04K
CQM1-ME04R
CQM1-ME08K
CQM1-ME08R



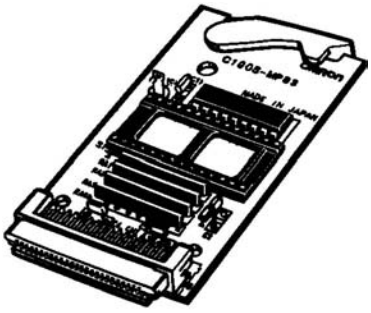
Flash Memory:

CQM1H-ME16K
CQM1H-ME16R



EPROM:

CQM1-MP08K
CQM1-MP08R



■ Available Memory Cassettes

The following Memory Cassettes are available.

Memory	Model	Specifications
EEPROM	CQM1-ME04K	4 Kwords without clock
	CQM1-ME04R	4 Kwords with clock
	CQM1-ME08K	8 Kwords without clock
	CQM1-ME08R	8 Kwords with clock
EPROM	CQM1-MP08K	Without clock (see below)
	CQM1-MP08R	With clock (see below)
Flash	CQM1H-ME16K	16 Kwords without clock
	CQM1H-ME16R	16 Kwords with clock

The following EPROM chips (sold separately) are required for EPROM Memory Cassettes.
The chip is mounted in the I/O socket on the Memory Cassette.

Model	ROM version	Capacity	Access speed
ROM-JD-B	27256 or equivalent	16 Kwords	150 ns
ROM-KD-B	27512 or equivalent	32 Kwords	150 ns

Specifications

■ General Specifications (Power Supplies and CPU Units)

Item	CQM1-PA203	CQM1-PA206	CQM1-PA216	CQM1-PD026
Supply voltage	100 to 240 V AC, 50/60 Hz		100 or 230 V AC (selectable), 50/60 Hz	24 V DC
Operating voltage range	85 to 264 V AC		85 to 132 V AC or 170 to 264 V AC	20 to 28 V DC
Operating frequency range	47 to 63 Hz			---
Power consumption	60 VA max.	120 VA max.		50 W max.
Inrush current	30 A max.			
Output capacity	5 V DC: 3.6 A (18 W)	5 V DC: 6 A 24 V DC: 0.5 A (30 W total)		5 V DC: 6 A (30 W)
Insulation resistance	20 MΩ min. (at 500 V DC) between AC external terminals and GR terminals (See note.)			
Dielectric strength	2,300 V AC 50/60 Hz for 1 min between AC external and GR terminals, leakage current: 10 mA max. (See note.) 1,000 V AC 50/60 Hz for 1 min between DC external and GR terminals, leakage current: 20 mA max. (See note.)			
Noise immunity	Conforms to IEC61000-4-4, 2 kV (power lines)			
Vibration resistance	10 to 57 Hz with an amplitude of 0.075 mm, and 57 to 150 Hz with an acceleration of 9.8 m/s^2 in the X, Y, and Z directions for 80 minutes each (i.e., swept for 8 minutes, 10 times).			
Shock resistance	147 m/s^2 (118 m/s^2 for Contact Output Units) 3 times each in X, Y, and Z directions			
Ambient temperature	Operating: 0 to 55 °C Storage: –20 to 75 °C (except battery)			
Ambient operating humidity	10% to 90% (no condensation)			
Operating environment	No corrosive gas			
Ground	Less than 100 Ω			
Construction	Panel mounted			
Weight	5 kg max.			
Internal current consumption	CQM1H-CPU11: 820 mA max. at 5 V DC CQM1H-CPU21/51/61: 840 mA max. at 5 V DC			
Dimensions (without cables)	CQM1H-CPU11/21: 187 to 571 × 110 × 107 mm (W×H×D) CQM1H-CPU51/61: 187 to 603 × 110 × 107 mm (W×H×D)			
Accessories	RS-232C connector (one XM2A-0901 Plug and one XM2S-0911-E Hood) (except CQM1H-CPU11) CPM2A-BAT01 Battery Set (installed in CPU Unit when shipped)			

Note: Disconnect the Power Supply Unit's LG terminal from the GR terminal when testing insulation and dielectric strength. Repeatedly testing the insulation and dielectric strength with the LG terminal and the GR terminals connected will damage internal circuits in the CPU Unit.

■ CPU Unit Specifications

Characteristics

Item		Specifications
Control method		Stored program method
I/O control method		Cyclic scan and direct output/immediate interrupt processing
Programming language		Ladder-diagram programming
I/O capacity		CQM1H-CPU11/21: 256 CQM1H-CPU51/61: 512
Program capacity		CQM1H-CPU11/21: 3.2 Kwords CQM1H-CPU51: 7.2 Kwords CQM1H-CPU61: 15.2 Kwords
Data memory capacity		CQM1H-CPU11/21: 3 Kwords CQM1H-CPU51: 6 Kwords CQM1H-CPU61: 12 Kwords (DM: 6 Kwords; EM: 6 Kwords)
Instruction length		1 step per instruction, 1 to 4 words per instruction
Number of instructions		162 (14 basic, 148 special instructions)
Instruction execution times		Basic instructions: 0.375 to 1.125 μs Special instructions: 17.7 μs (MOV instruction)
Overseeing time		0.70 ms
Mounting structure		No Backplane (Units are joined horizontally using connectors)
Mounting		DIN Track mounting (screw mounting not possible)
CPU Unit built-in DC input points		16
Maximum number of Units		CPU Block only: 11 Units (I/O Units and Dedicated I/O Units) max. CPU Block and Expansion I/O Block CPU Block: 5 Units max. Expansion I/O Block: 11 Units max.
Inner Boards		CQM1H-CPU11/21: None CQM1H-CPU51/61: 2 Boards
Communications Units (Controller Link Unit)		CQM1H-CPU11/21: None CQM1H-CPU51/61: 1 Unit
Types of interrupts	Input interrupts (4 inputs max.)	Input Interrupt Mode: Interrupts are executed in response to inputs from external sources to the CPU Unit's built-in input points. Counter Mode: Interrupts are executed in response to reception of a set number of pulses (counted down) via the CPU Unit's internal built-in input points (4 points).
	Interval timer interrupts (3 timers max.)	Scheduled Interrupt Mode: Program is interrupted at regular intervals measured by one of the CPU Unit's internal timers. One-shot Interrupt Mode: An interrupt is executed after a set time, measured by one of the CPU Unit's internal timers.
	High-speed counter interrupts	Target Value Comparison: Interrupt is executed when the high-speed counter PV is equal to a specified value. Range Comparison: Interrupt is executed when the high-speed counter PV lies within a specified range. **Note:** Counting is possible for high-speed counter inputs from the CPU Unit's internal input points, Pulse I/O Boards, or Absolute Encoder Interface Boards. (The High-speed Counter Board has no interrupt function, but can output bit patterns internally and externally.)
I/O allocations		I/O is automatically allocated in order from the Unit nearest to the CPU Unit. (Because there are no I/O tables, it is not necessary, and not possible, to create I/O tables from a Programming Device.)

Note: Analog Power Supply Units must also be counted.

Memory Area Structure

Data area		Size	Words	Bits	Function
IR area	Input area	256 bits	IR 000 to IR 015	IR 00000 to IR 01515	Input bits are allocated to Input Units or Dedicated I/O Units. The 16 bits in IR 000 are always allocated to the CPU Unit's built-in inputs. Bits in IR 001 to IR 015 are allocated to I/O or Dedicated I/O Units connected to the CPU Unit.
	Output area	256 bits	IR 100 to IR 115	IR 10000 to IR 11515	Output bits are allocated to Output Units or Dedicated I/O Units connected to the CPU Unit.
	Work areas	2,528 bits min.	IR 016 to IR 089	IR 01600 to IR 08915	Work bits do not have any specific function and they can be freely used within the program. (A minimum 2,528 bits are available as work bits. Most bits in the IR and LR areas can be used as work bits when they are not used for their allocated functions, so the total number of available work bits depends on the configuration of the PLC.)
			IR 116 to IR 189	IR 11600 to IR 18915	
			IR 216 to IR 219	IR 21600 to IR 21915	
			IR 224 to IR 229	IR 22400 to IR 22915	
Controller Link status areas		96 bits	IR 090 to IR 095	IR 09000 to IR 09515	Status Area 1: Stores the Controller Link data link status information.
		96 bits	IR 190 to IR 195	IR 19000 to IR 19515	Status Area 2: Stores the Controller Link error and network participation information.
MACRO operand area	Input area	64 bits	IR 096 to IR 099	IR 09600 to IR 09915	Used when the MACRO instruction, MCRO(99), is used.
	Output area	64 bits	IR 196 to IR 199	IR 19600 to IR 19915	
Inner Board slot 1 area		256 bits	IR 200 to IR 215	IR 20000 to IR 21515	These bits are allocated to the Inner Board mounted in slot 1 of a CQM1H-CPU51/61. High-speed Counter Board: IR 200 to IR 213 Serial Communications Board: IR 200 to IR 207
Analog settings area		64 bits	IR 220 to IR 223	IR 22000 to IR 22315	Used to store the analog settings when a CQM1H-AVB41 Analog Setting Board is mounted.
High-speed Counter 0 PV		32 bits	IR 230 to IR 231	IR 23000 to IR 23115	Used to store the present values of high-speed counter 0.
Inner Board slot 2 area		192 bits	IR 232 to IR 243	IR 23200 to IR 24315	These bits are allocated to the Inner Board mounted in slot 2. High-speed Counter Board: IR 232 to IR 243 Absolute Encoder Interface Board: IR 232 to IR 239 Pulse I/O Board: IR 232 to IR 239 Analog I/O Board: IR 232 to IR 239
SR area		184 bits	SR 244 to SR 255	SR 24400 to SR 25507	These bits serve specific functions such as flags and control bits.
HR area		1,600 bits	HR 00 to HR 99	HR 0000 to HR 9915	These bits store data and retain their ON/OFF status when power is turned OFF or when the operating mode is changed.
AR area		448 bits	AR 00 to AR 27	AR 0000 to AR 2715	These bits serve specific functions such as flags and control bits.
TR area		8 bits	---	TR 0 to TR 7	These bits are used to temporarily store ON/OFF status at program branches.
LR area		1,024 bits	LR 00 to LR 63	LR 0000 to LR 6315	Used for 1:1 data link through the RS-232 port or through a Controller Link Unit.
Timer/Counter area		512 bits	TIM/CNT 000 to TIM/CNT 511 (timer/counter numbers)		The same numbers are used for both timers and counters. Timer numbers 000 to 015 can be used with TIMH(15) for interrupt-refreshed PVs to ensure proper timing without inaccuracy being caused by the cycle time.

Data area		Size	Words	Bits	Function
DM area	Read/ write	3,072 words	DM 0000 to DM 3071	---	DM area data can be accessed in word units only. Word values are retained when the power is turned OFF.
		3,072 words	DM 3072 to DM 6143	---	Available in CQM1H-CPU51/61 CPU Units only.
	Read-only[4]	425 words	DM 6144 to DM 6568	---	Cannot be written from the program (only from a Programming Device). DM 6400 to DM 6409: Controller Link parameters DM 6450 to DM 6499: Routing tables DM 6550 to DM 6559: Serial Communications Board Setup
	Error history area[4]	31 words	DM 6569 to DM 6599	---	Cannot be written from the program (only from a Programming Device). Stores the time of occurrence and error code of errors that occur.
	PLC Setup[4]	56 words	DM 6600 to DM 6655	---	Cannot be written from the program (only from a Programming Device). Stores various parameters that control PLC operation.
EM area		6,144 words	EM 0000 to EM 6143	---	EM area data can be accessed in word units only. Word values are retained when the power is turned OFF or the operating mode is changed. (CQM1H-CPU61 CPU Unit only.)

Memory Cassette Specifications

Item	Details
Memory Cassette (EEPROM or flash memory)	Mounted from the front of the CPU Unit and used to store and read the user's program, DM (read-only DM and PLC Setup), and expansion instruction information as one block. It is possible to set the CPU Unit so that data stored in the Memory Cassette (user's program, DM, expansion instruction information) is automatically sent to the CPU Unit (autoboot) at startup. Transfer and comparison of data between the CPU Unit and Memory Cassette are possible using AR area control bits.

Other Functions

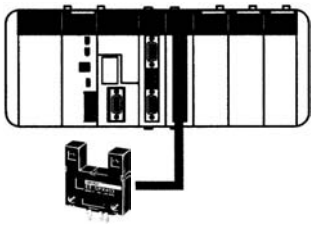
Item	Specification
Macro instructions	Subroutines called by instructions containing arguments.
Min. cycle time	1 to 9,999 ms (Unit: 1 ms)
Cycle time monitoring	When the cycle time exceeds 100 ms, the Cycle Time Over Flag turns ON, and operation continues. (A setting can be made in the PLC Setup so that this error is not generated.) When the cycle time exceeds the cycle monitor time, operation is stopped. Cycle monitor time settings: 0 to 990 ms in 10-ms units, 0 to 9,900 ms in 100-ms units, 0 to 99 s in 1-s units. **Note:** The maximum and current values of the cycle time are stored in the AR area.
I/O refreshing	Cyclic refreshing, refreshing by IORF(97), direct output refreshing (set in the PLC Setup), interrupt input refreshing. (The inputs that are refreshed can be set separately for input interrupts, high-speed counter interrupts, and interval timer interrupts in the PLC Setup.)
I/O memory status when changing operating mode	Depends on the ON/OFF status of the I/O Hold Bit (SR 25212).
Load OFF	All outputs on Output Units can be turned OFF when the CPU Unit is operating in RUN, MONITOR, or PROGRAM mode. (Used for stopping output in emergencies, for debugging, etc.)
User-customized DIP switch setting	A pin setting on the DIP switch on the front of the CPU Unit is stored in AR 0712. This setting can be used as an ON/OFF condition (e.g., to switch between trial operation and actual operation).
Mode setting at power-up	Possible
Debugging	Forced set/reset, differential monitoring, data tracing (scheduled, cyclic, or when instruction is executed).
Online editing	User programs can be overwritten in program-block units when the CPU Unit is in MONITOR mode. With the CX-Programmer, more than one program block can be edited at the same time.
Program protection	Write-protection of user program and data memory (DM 6144 to DM 6655: read-only DM): Set using pin 1 of the DIP switch.
Error check	User-defined errors (i.e., user can define fatal errors and non-fatal errors using the FAL(06) and FALS(07) instructions.) (It is possible to stop operation using FALS(07) for fatal errors. User-defined error logs can be created in specific bits (logging) when using FAL(06).
Error log	Up to 10 errors (including user-defined errors) are stored in the error log. Information includes the error code, error details, and the time the error occurred.

Item	Specification			
Serial communications	Built-in peripheral port: Programming Device (including Programming Console) connections, Host Links, no-protocol communications Built-in RS-232C port: Programming Device (excluding Programming Console) connections, Host Links, no-protocol communications, NT Links (1:1 mode), 1:1 Data LInks			
	RS-232C port and RS-422A/485 port on Serial Communications Board (sold separately): Programming Device (excluding Programming Console) connections, Host Links, no-protocol communications, NT Links (1:1 mode, 1:N mode), 1:1 Data LInks, protocol macros			
Serial communications modes	CQM1H CPU Unit's built-in port	Built-in peripheral port	Built-in RS-232C port	Serial Communications Board ports
Programming Console bus	Connects to Programming Console.	YES (pin 7 OFF)	No	No
Peripheral bus	Connects to a computer running CX-Programmer or other Support Software. (Automatically used if the network type is set to peripheral bus on the Support Software.)	YES (pin 7 ON)	No	No
Host Link (SYSMAC WAY)	Enables reading/writing CPU Unit I/O memory or program using Host Link commands. Computers running Support Software or OMRON Programmable Terminals can also be connected. PLC-initiated communications are possible.	YES (pin 7 ON)	YES	YES
No-protocol	Enables sending or receiving up to 256 bytes of data without a protocol or data conversion. A start code, end code, and transmission delay can be set.	YES (pin 7 ON)	YES	YES
1:1 data link	Enables 1:1 data link with a CQM1H, CQM1, CPM-series, C200HX/HG/HE, C200HS, or SRM1 PLC.	No	YES	YES
NT links (1:1 and 1:N)	Enables 1:1 or 1:N communications with OMRON Programmable Terminals without additional programming.	No	YES (1:1 only)	YES (1:1 and 1:N)
Protocol macros	Enables user-created protocols to communicate with essential any device equipped with a serial communications port (e.g., RS-232C). Standard protocols are also provided.	No	No	YES
Clock	Some Memory Cassette are equipped with a clock. (The time of the error will recorded if a clock is used.			
Input time constants	Used to set the ON (or OFF) response times for DC Input Units. Settings: 1, 2, 4, 8, 16, 32, 64, and 128 ms.			
Power OFF detection time	AC power supply: 10 to 25 ms (not fixed), DC power supply: 5 to 25 ms (not fixed)			
Memory protection	Held Areas: Holding bits, contents of Data Memory and Extended Data Memory, and status of the counter Completion Flags and present values. **Note:** If the I/O Hold Bit (SR 25212) is turned ON, and the PLC Setup is set to maintain the I/O Hold Bit status when power is turned ON, the contents of the IR area and the LR area will be saved.			
Commands to a host computer	Host Link command responses can be sent to a computer connected via the Host Link System using the TXD(—) (communications port output) instruction.			
Remote programming and monitoring	Host Link or peripheral bus communications via a CPU Unit's serial communications port can be used for remote programming and remote monitoring of the PLC through a Controller Link System. (This function is, however, not supported for the serial communications ports on the Serial Communications Board.)			
Program check	Program is checked at the beginning of operation for items such as no END(01) instruction and instruction errors. CX-Programmer can also check programs. (The level of program checking can be set.)			
Battery life	5 years at 25°C (Depends on the ambient temperature and power supply conditions. Min.: 1 yr) Battery replacement must be performed within 5 minutes.			
Errors from self-diagnostics	CPU (watchdog timer), I/O verification, I/O bus, memory, FALS system (FALS execution or cycle monitor time over), FAL system (FAL execution or PLC Setup error etc.), battery, cycle time over and communications port.			
Other functions	Storage of number of times power has been interrupted. (Stored in AR area.)			

I/O Functions

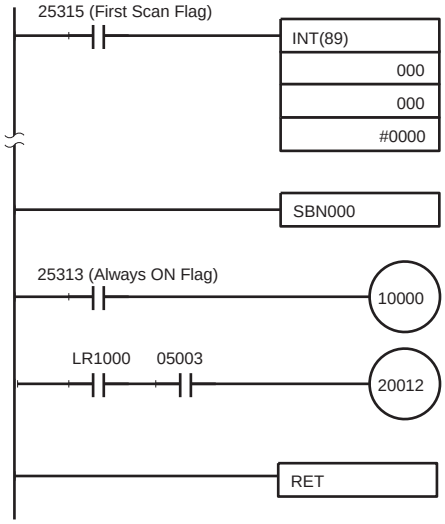
■ Interrupt Input Processing

All CQM1H CPU Units are equipped with four inputs (IR 00000 to IR 00003) that can be used as interrupt inputs. Interrupt processing can be enabled and disabled with the INTERRUPT CONTROL – INT(89) instruction.



Photomicrosensor etc.

Sample Program



In order for interrupt input processing to be performed, the INTERRUPT CONTROL – INT(89) instruction is set so that interrupt processing is enabled when IR 00000 goes ON.

When the external signal to IR 00000 goes from OFF to ON, program execution is temporarily halted, and processing moves to subroutine 00.

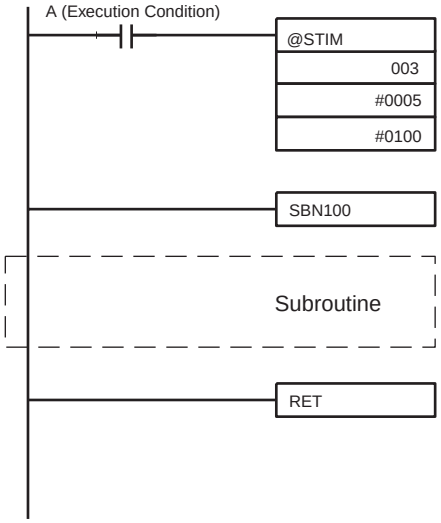
When subroutine 000 (SBN000) is completed, its results are output immediately. The entire interrupt process, from IR 00000 going ON to the refreshing of outputs IR 10000 and IR 20012, provides high-speed I/O response that is not affected by the PLC's cycle time.

■ Interval Timer Interrupt Processing

The INTERVAL TIMER – STIM(69) instruction is useful for performing repetitive processes, such as output processing, that need to be performed regularly at intervals shorter than the cycle time.

Place an STIM(69) instruction in the program to define a timer that will call and execute a subroutine at regular intervals. Up to 3 interval timers can be used.

Sample Program



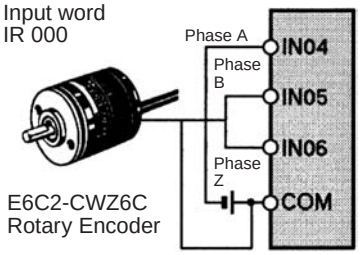
The STIM(69) instruction is used to control an interval timer. In this example, timer 0 is started in repetitive mode.

As long as A (the execution condition) is ON, the main program will be halted and the interrupt routine SBN100 will executed every 5 ms (i.e., each time the interval timer times out). Main program execution is continued when interrupt routine execution has been completed.

Various I/O Functions

■ Internal High-speed Counters

Pulses from a rotary encoder can be input directly into 3 of the CPU Unit's inputs (IN04, IN05, and IN06) and used as internal high-speed counter.
Pulses can be counted from 0 to 65535 in the increment mode and –32767 to 32767 in the up/down mode, with a single-phase response speed of 5 KHz and a two-phase response speed of 2.5 KHz.



The high-speed counter's input mode is set in the DM Area's PLC Setup.

Input Modes

Up/Down mode	Uses phase A and phase B to count up and down.
Increment mode	Uses phase A only to count up.
Normal mode	Input bit 04 to bit 06 are used as normal inputs.

Reset Method

There are two ways to reset the counter's PV. The PV can be reset by the software reset alone or by a logical AND between the phase-Z input and the software reset.

Comparison Conditions

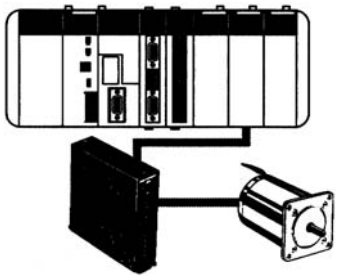
Target value	Up to 16 target values can be set. The specified subroutine will be executed when the count value reaches a target value.
Zone comparison	Up to 8 zones (upper/lower limits) can be set. The specified subroutine will be executed when the count value is within a zone.

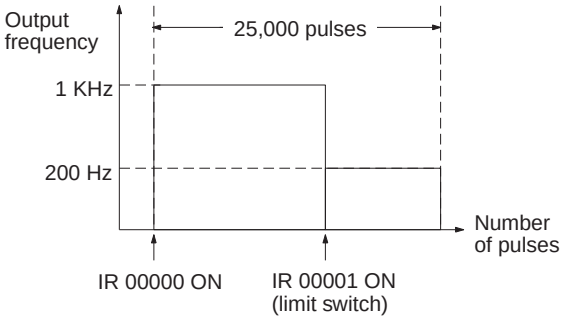
■ Pulse Output - PULS(65) and Change Frequency - SPED(64)

These instructions are used to control pulse outputs. They can greatly simplify tasks such as controlling step motors from the CQM1H.

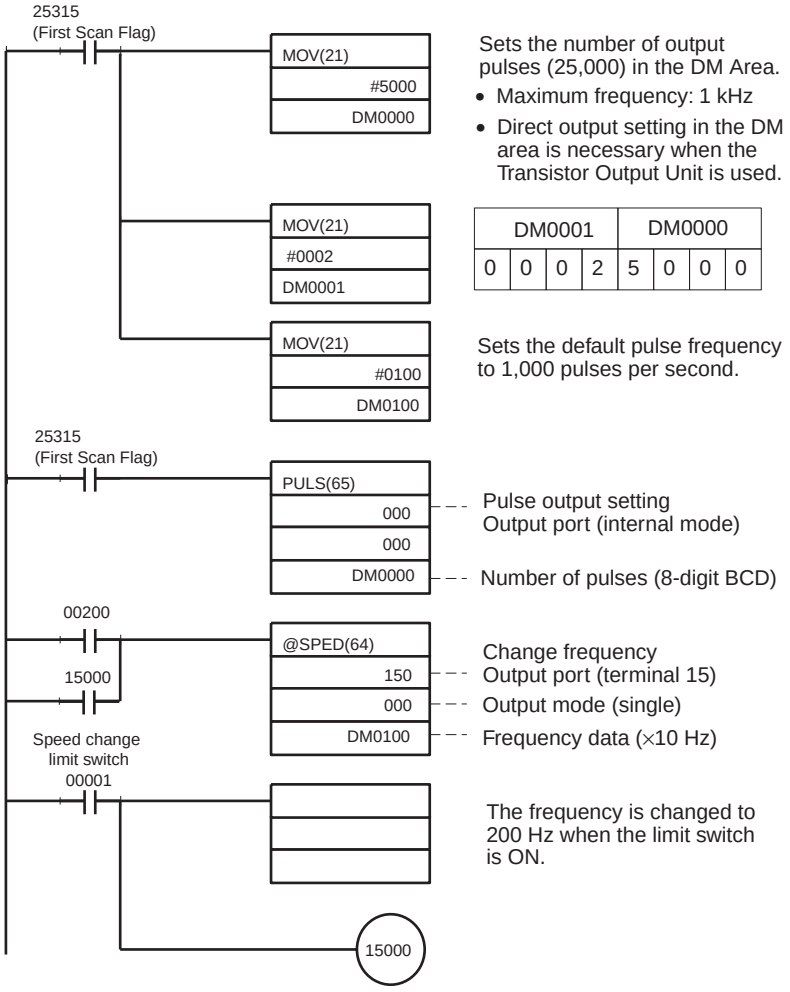
Example

In this example, the speed of a step motor is changed.





Sample Program



I/O Memory Allocation

I/O words are allocated to I/O Units according to a fixed location. When the I/O Units and Dedicated I/O Units are connected, the I/O words will be allocated as described next.

Input Word Allocation

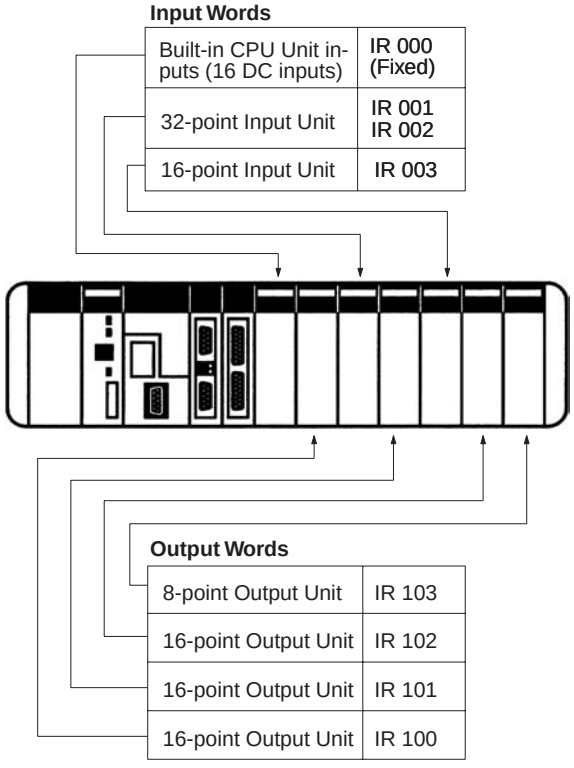
IR 000 to IR 015 are allocated as input bits. The first input word (IR 000), however, is allocated to the CPU Unit's 16 built-in input points.

Note: Built-in CPU Unit's inputs are used for interrupt processing and built-in high-speed counter inputs.

Output Word Allocation

IR 100 to IR 115 are allocated as output bits. When Output Units or Dedicated I/O Units are connected, words will be allocated in order starting from IR 100.

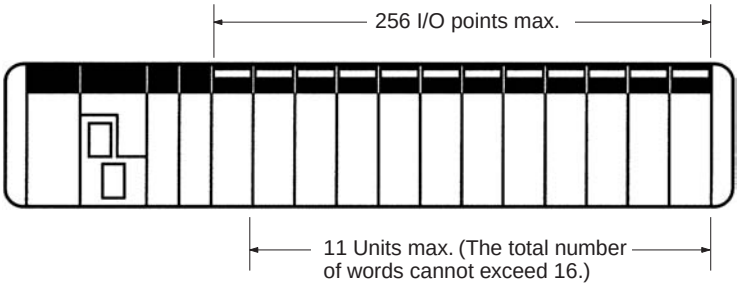
Unit		I/O word allocation		
		Input words	Output words	
Input Units		1 or 2	---	Each 8-point or 16-point Input Unit is allocated one input word and each 32-point Input Unit is allocated two input words. Words will be allocated in order starting from IR 001.
Output Units		---	1 or 2	Each 8-point or 16-point Output Unit is allocated one output word and each 32-point Output Unit is allocated two output words. Words will be allocated in order starting from IR 100.
Sensor Units		1	---	Each Sensor Unit is allocated one input word. Bits 00 through 03 are allocated in order from the top to a maximum of four modules. All other bits can be used as work bits in programming.
B7A Interface Units	B7A02	---	1	Depending on the Unit, each B7A Interface Unit is allocated input words and output words.
	B7A12	1	---	
	B7A03	---	1	
	B7A13	2	---	
	B7A21	1	1	
DeviceNet I/O Link Unit		1	1	Each DeviceNet I/O Link Unit is allocated one input word and one output word.
CompoBus/S Master Units	IN:16 points OUT: 16 points	1	1	Depending on the Unit, each CompoBus/S Master Unit is allocated input words and output words.
	IN: 32 points OUT: 32 points	2	2	
	IN: 64 points OUT: 64 points	4	4	
Analog Input Unit		2 or 4	---	Each Analog Input Unit can be set to input either 2 or 4 points. If the Unit is set to input 2 points, two input words are allocated. If the Unit is set to input 4 points, four input words are allocated.
Analog Output Unit		---	2	Each Analog Output Unit is allocated two output words.
Analog Power Supply Units		---	---	Power Supply Units are not involved directly in I/O operations and are thus not allocated I/O words.
Temperature Control Units	00□/10□	2 or 1	2 or 1	Each Temperature Control Unit is allocated two input words and two output words when two loops are used. Only one input word and one output word are allocated when one loop is used.
	20□/30□	1	1	One input word and one output word are allocated in the order the Unit is connected.
Safety Relay Unit		1	---	One input word is allocated per Unit in the order the Unit is connected.



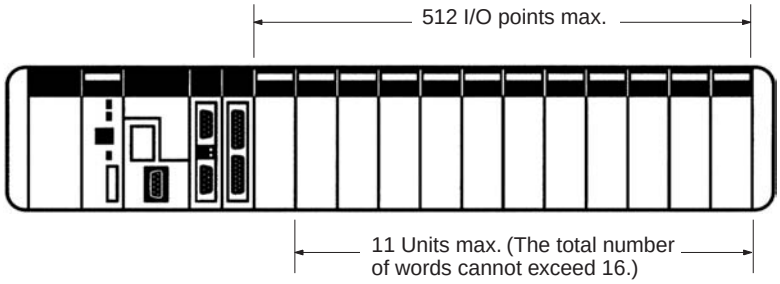
I/O Units

The number of I/O Units that can be connected depends on the CPU Unit being used.

CQM1H-CPU11/CPU21



CQM1H-CPU51/CPU61



Instructions

■ Sequence Instructions

Sequence Input Instructions

Name	Mnemonic	Code
LOAD	LD	Note 1.
LOAD NOT	LD NOT	
AND	AND	
AND NOT	AND NOT	
OR	OR	
OR NOT	OR NOT	
AND LOAD	AND LD	
OR LOAD	OR LD	

Sequence Output Instructions

Name	Mnemonic	Code
OUTPUT	OUT	Note 1.
OUT NOT	OUT NOT	Note 1.
KEEP	KEEP	11
DIFFERENTIATE UP	DIFU	13
DIFFERENTIATE DOWN	DIFD	14
SET	SET	Note 1.
RESET	RSET	Note 1.

Sequence Control Instructions

Name	Mnemonic	Code
END	END	01
NO OPERATION	NOP	00
INTERLOCK	IL	02
INTERLOCK CLEAR	ILC	03
JUMP	JMP	04
JUMP END	JME	05

■ Timer/Counter Instructions

Name	Mnemonic	Code
TIMER	TIM	Note 1.
HIGH-SPEED TIMER	TIMH	15
TOTALIZING TIMER	TTIM	Note 2/3.
COUNTER	CNT	Note 1.
REVERSIBLE COUNTER	CNTR	12

■ Data Comparison Instructions

Name	Mnemonic	Code
COMPARE	CMP	20
DOUBLE COMPARE	CMPL	(60: Note 2)
SIGNED BINARY COMPARE	CPS	Note 2.
SIGNED BINARY DOUBLE COMPARE	CPSL	Note 2.
MULTI-WORD COMPARE	(@)MCMP	(19: Note 2)
TABLE COMPARE	(@)TCMP	85
BLOCK COMPARE	(@)BCMP	(68: Note 2)
RANGE COMPARE	ZCP	Note 2
RANGE DOUBLE COMPARE	ZCPL	Note 2

■ Data Movement Instructions

Name	Mnemonic	Code
MOVE	(@)MOV	21
MOVE NOT	(@)MVN	22
MOVE BIT	(@)MOVB	82
MOVE DIGIT	(@)MOVD	83
MULTIPLE BIT TRANSFER	(@)XFRB	Note 2.
BLOCK TRANSFER	(@)XFER	70
BLOCK SET	(@)BSET	71
DATA EXCHANGE	(@)XCHG	73
SINGLE WORD DISTRIBUTE	(@)DIST	80
DATA COLLECT	(@)COLL	81

■ Data Shift Instructions

Name	Mnemonic	Code
SHIFT REGISTER	SFT	10
REVERSIBLE SHIFT REGISTER	(@)SFTR	84
ONE DIGIT SHIFT LEFT	(@)SLD	74
ONE DIGIT SHIFT RIGHT	(@)SRD	75
ASYNCHRONOUS SHIFT REGISTER	(@)ASFT	(17: Note 2)
WORD SHIFT	(@)WSFT	16
ARITHMETIC SHIFT LEFT	(@)ASL	25
ARITHMETIC SHIFT RIGHT	(@)ASR	26
ROTATE LEFT	(@)ROL	27
ROTATE RIGHT	(@)ROR	28

■ Increment/Decrement Instructions

Name	Mnemonic	Code
INCREMENT	(@)INC	38
DECREMENT	(@)DEC	39

Note: 1. Input via Programming Console Key.

2. Expansion instruction (function code set before programming).

3. New (i.e., not supported by CQM1).

4. Supported by CQM1H CPU Units with lot number 0160 (June 1, 2000) or later.

■ Arithmetic Instructions

Name	Mnemonic	Code
BCD ADD	(@)ADD	30
BCD SUBTRACT	(@)SUB	31
DOUBLE BCD ADD	(@)ADDL	54
DOUBLE BCD SUBTRACT	(@)SUBL	55
BINARY ADD	(@)ADB	50
BINARY SUBTRACT	(@)SBB	51
BINARY DOUBLE ADD	(@)ADBL	Note 2.
BINARY DOUBLE SUBTRACT	(@)SBBL	Note 2.
BCD MULTIPLY	(@)MUL	32
DOUBLE BCD MULTIPLY	(@)MULL	56
BINARY MULTIPLY	(@)MLB	52
SIGNED BINARY MULTIPLY	(@)MBS	Note 2.
SIGNED BINARY DOUBLE MULTIPLY	(@)MBSL	Note 2.
BCD DIVIDE	(@)DIV	33
DOUBLE BCD DIVIDE	(@)DIVL	57
BINARY DIVIDE	(@)DVB	53
SIGNED BINARY DIVIDE	(@)DBS	Note 2.
SIGNED BINARY DOUBLE DIVIDE	(@)DBSL	Note 2.

■ Data Conversion Instructions

Name	Mnemonic	Code
BCD TO BINARY	(@)BIN	23
DOUBLE BCD TO DOUBLE BINARY	(@)BINL	58
BINARY TO BCD	(@)BCD	24
DOUBLE BINARY TO DOUBLE BCD	(@)BCDL	59
2'S COMPLEMENT CONVERT	(@)NEG	Note 2
2'S COMPLEMENT DOUBLE CONVERT	(@)NEGL	Note 2
4 TO 16 DECODER	(@)MLPX	76
16 TO 4 ENCODER	(@)DMPX	77
ASCII CODE CONVERT	(@)ASC	86
ASCII TO HEXADECIMAL	(@)HEX	Note 2
COLUMN TO LINE	(@)LINE	Note 2
LINE TO COLUMN	(@)COLM	Note 2

■ Logic Instructions

Name	Mnemonic	Code
LOGICAL AND	(@)ANDW	34
LOGICAL OR	(@)ORW	35
EXCLUSIVE OR	(@)XORW	36
EXCLUSIVE NOR	(@)XNRW	37
COMPLEMENT	(@)COM	29

■ Special Math Instructions

Name	Mnemonic	Code
ARITHMETIC PROCESS	(@)APR	Note 2
BIT COUNTER	(@)BCNT	(67: Note 2)
SQUARE ROOT	(@)ROOT	72

■ Floating-point Math and Conversion Instructions

Name	Mnemonic	Code
FLOATING TO 16-BIT	(@)FIX	Note 2/3
FLOATING TO 32-BIT	(@)FIXL	
16-BIT TO FLOATING	(@)FLT	
32-BIT TO FLOATING	(@)FLTL	
FLOATING-POINT ADD	(@)+F	
FLOATING-POINT SUBTRACT	(@)–F	
FLOATING-POINT MULTIPLY	(@)*F	
FLOATING-POINT DIVIDE	(@)/F	
DEGREES TO RADIANS	(@)RAD	
RADIANS TO DEGREES	(@)DEG	
SINE	(@)SIN	
COSINE	(@)COS	
TANGENT	(@)TAN	
ARC SINE	(@)ASIN	
ARC COSINE	(@)ACOS	
ARC TANGENT	(@)ATAN	
SQUARE ROOT	(@)SQRT	
EXPONENT	(@)EXP	
LOGARITHM	(@)LOG	

■ Table Data Instructions

Name	Mnemonic	Code
DATA SEARCH	(@)SRCH	Note 2
FIND MAXIMUM	(@)MAX	
FIND MINIMUM	(@)MIN	
SUM CALCULATE	(@)SUM	
FCS CALCULATE	(@)FCS	

■ Data Control Instructions

Name	Mnemonic	Code
PID CONTROL	PID	Note 2
SCALE	(@)SCL	(66: Note 2)
SCALE 2	(@)SCL2	Note 2
SCALE 3	(@)SCL3	Note 2
AVERAGE VALUE	AVG	Note 2

Note: 1. Input via Programming Console Key.

2. Expansion instruction (function code set before programming).

3. New (i.e., not supported by CQM1).

4. Supported by CQM1H CPU Units with lot number 0160 (June 1, 2000) or later.

■ Subroutine Instructions

Name	Mnemonic	Code
SUBROUTINE ENTER	(@)SBS	91
SUBROUTINE ENTRY	SBN	92
SUBROUTINE RETURN	RET	93
MACRO	(@)MCRO	99

■ Interrupt Instructions

Name	Mnemonic	Code
INTERRUPT CONTROL	(@)INT	(89: Note 2)
INTERVAL TIMER	(@)STIM	(69: Note 2)

■ High-speed Counter and Pulse Output Instructions

Name	Mnemonic	Code
MODE CONTROL	(@)INI	(61: Note 2)
PV READ	(@)PRV	(62: Note 2)
COMPARE TABLE LOAD	(@)CTBL	(63: Note 2)
SET PULSE	(@)PULS	(65: Note 2)
CHANGE FREQUENCY	(@)SPED	(64: Note 2)
FREQUENCY CONTROL	(@)ACC	Note 2
POSITIONING	(@)PLS2	Note 2
PWM OUTPUT	(@)PWM	Note 2

■ Step Instructions

Name	Mnemonic	Code
STEP DEFINE	STEP	08
STEP START	SNXT	09

■ I/O Unit Instructions

Name	Mnemonic	Code
I/O REFRESH	(@)IORF	97
7-SEGMENT DECODER	(@)SDEC	78
7-SEGMENT DISPLAY OUTPUT	7SEG	(88: Note 2)
DIGITAL SWITCH	DSW	(87: Note 2)
TEN KEY INPUT	(@)TKY	(18: Note 2)
HEXADECIMAL KEY INPUT	HKY	Note 2

■ Serial Communications Instructions

Name	Mnemonic	Code
PROTOCOL MACRO	(@)PMCR	Note 2/3
TRANSMIT	(@)TXD	(48: Note 2)
RECEIVE	(@)RXD	(47: Note 2)
CHANGE SERIAL PORT SETUP	(@)STUP	Note 2/3

■ Network Communications Instructions

Name	Mnemonic	Code
NETWORK SEND	(@)SEND	90 (Note 3)
NETWORK RECEIVE	(@)RECV	98 (Note 3)
DELIVER COMMAND	(@)CMND	Note 2/3

■ Message Instructions

Name	Mnemonic	Code
MESSAGE	(@)MSG	46

■ Clock Instructions

Name	Mnemonic	Code
HOURS TO SECONDS	(@)SEC	Note 2
SECONDS TO HOURS	(@)HMS	Note 2

■ Debugging Instructions

Name	Mnemonic	Code
TRACE MEMORY SAMPLE	TRSM	45

■ Diagnostic Instructions

Name	Mnemonic	Code
FAILURE ALARM	(@)FAL	06
SEVERE FAILURE ALARM	FALS	07
FAILURE POINT DETECT	FPD	Note 2

■ Carry Flag Instructions

Name	Mnemonic	Code
SET CARRY	(@)STC	40
CLEAR CARRY	(@)CLC	41

■ Temperature Control Unit Instructions

Name	Mnemonic	Code
TRANSFER I/O COMMAND	IOTC	Note 2/4

Note: 1. Input via Programming Console Key.

2. Expansion instruction (function code set before programming).

3. New (i.e., not supported by CQM1).

4. Supported by CQM1H CPU Units with lot number 0160 (June 1, 2000) or later.

I/O Specifications

■ Input Specifications

All of the Input Units listed in the following tables have photocoupler isolation and LED input indicators.

CPU Units

Number of inputs	Input voltage	Input current	Input impedance	Operating voltage		Response times		External connection	Inputs/ common	Current consumption (5 V DC)	Weight
				ON voltage	OFF voltage	ON delay	OFF delay				
16 pts	24 V DC +10%/15%	10 mA for IN04/05 6 mA for the rest (24 V DC)	2.2 kΩ for IN04/05 3.9 kΩ for the rest	17.4 V DC min.	5.0 V DC max.	8 ms max. (see note)	8 ms max. (see note)	Terminal block	16	---	---

DC Input Units

Model	Number of inputs	Input voltage	Input current	Input impedance	Operating voltage		Response times		External connection	Inputs/ common	Current consumption (5 V DC)	Weight
					ON voltage	OFF voltage	ON delay	OFF delay				
CQM1-ID211	8 pts	12 to 24 V DC +10%/15%	10 mA (24 V DC)	2.4 kΩ	10.2 V DC min.	3.0 V DC max.	8 ms max. (see note)	8 ms max. (see note)	Terminal block	8 independent commons	50 mA max.	180 g max.
CQM1-ID111	16 pts	12 V DC +10%/15%	6 mA (12 V DC)	1.8 kΩ	8.0 V DC min.	3.0 V DC max.	8 ms max. (see note)	8 ms max. (see note)		16	85 mA max.	180 g max.
CQM1-ID212	16 pts	24 V DC +10%/15%	6 mA (24 V DC)	3.9 kΩ	14.4 V DC min.	5.0 V DC max.	8 ms max. (see note)	8 ms max. (see note)		16	85 mA max.	180 g max.
CQM1-ID112	32 pts	12 V DC +10%/15%	4 mA (12 V DC)	2.2 kΩ	8.0 V DC min.	3.0 V DC max.	8 ms max. (see note)	8 ms max. (see note)	Connector	32	170 mA max.	160 g max.
CQM1-ID213	32 pts	24 V DC +10%/15%	4 mA (24 V DC)	5.6 kΩ	14.4 V DC min.	5.0 V DC max.	8 ms max. (see note)	8 ms max. (see note)		32	170 mA max.	160 g max.
CQM1-ID214	32 pts	24 V DC +10%/15%	6 mA (24 V DC)	3.9 kΩ	15.4 V DC min.	5.0 V DC max.	8 ms max. (see note)	8 ms max. (see note)		32	170 mA max.	160 g max.

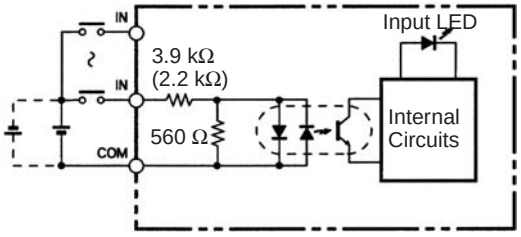
AC Input Units

Model	Number of inputs	Input voltage	Input current	Input impedance	Operating voltage		Response times		External connection	Inputs/ common	Current consumption (5 V DC)	Weight
					ON voltage	OFF voltage	ON delay	OFF delay				
CQM1-IA121	8 pts	100 to 120 V AC +10%/15%	5 mA (100 V AC)	20 kΩ (50 Hz) 17 kΩ (60 Hz)	60 V AC min.	20 V AC max.	35 ms max.	55 ms max.	Terminal block	8	50 mA max.	210 g max.
CQM1-IA221	8 pts	200 to 240 V AC +10%/15%	6 mA (200 V AC)	38 kΩ (50 Hz) 32 kΩ (60 Hz)	150 V AC min.	40 V AC max.	35 ms max.	55 ms max.		8	50 mA max.	210 g max.

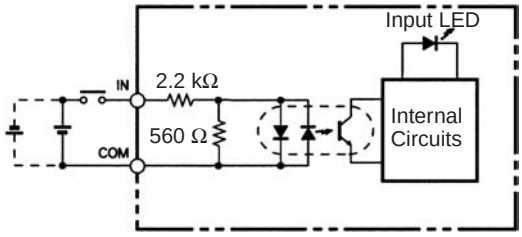
Note: Selectable from 1 to 128 ms in the PLC Setup.

■ Circuit Configuration

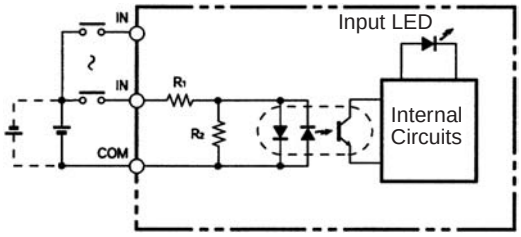
CQM1H-CPU11/21/51/61



CQM1-ID211

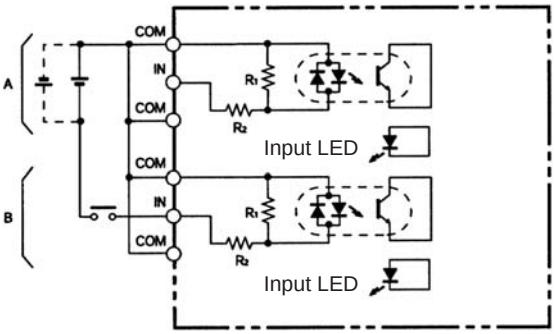


CQM1-ID111/212



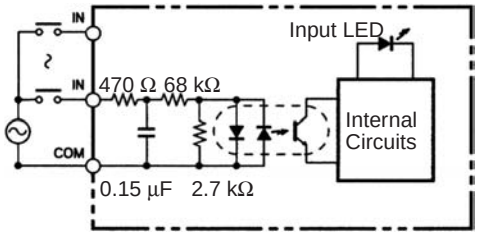
ID111
R_1: 1.8 kΩ
R_2: 620 Ω
ID211
R_1: 3.9 kΩ
R_2: 560 Ω

CQM1-ID112/213/214

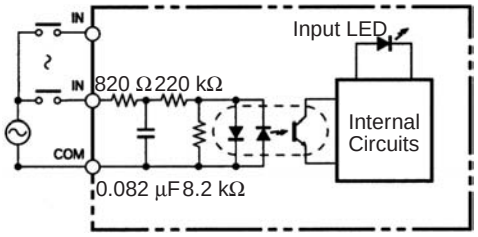


ID112
R_1: 750 Ω
R_2: 2.2 kΩ
ID213
R_1: 620 Ω
R_2: 5.6 kΩ
ID214
R_1: 620 Ω
R_2: 3.9 kΩ

CQM1-IA121



CQM1-IA221



■ Output Unit Specifications

All of the Output Units have LED output indicators.

Contact Output Units

Model	Number of outputs	Max. switching capacity	Min. switching capacity	Response times		External connector	Leakage current	Outputs/ common	Fuses (see note)	External power supply capacity	Internal current consumption (5 V DC)	Weight
				ON delay	OFF delay							
CQM1-OC221	8 pts	2 A, 250 V AC (cosϕ= 1) 2 A, 250 V AC (cosϕ= 0.4) 2 A, 24 V DC (16 A/Unit)	10 mA, 5 V DC	10 ms max.	5 ms max.	Terminal block	---	Independent commons	None	---	430 mA max.	200 g max.
CQM1-OC222	16 pts	2 A, 250 V AC (cosϕ= 1) 2 A, 250 V AC (cosϕ= 0.4) 2 A, 24 V DC (8 A/Unit)	10 mA, 5 V DC	10 ms max.	5 ms max.			16		---	850 mA max.	230 g max.
CQM1-OC224	8 pts	2 A, 250 V AC (cosϕ= 1) 2 A, 250 V AC (cosϕ= 0.4) 2 A, 24 V DC (16 A/Unit)	10 mA, 5 V DC	15 ms max.	5 ms max.			Independent commons		---	440 mA max.	270 g max.

Transistor Output Units

Model	Number of outputs	Max. switching capacity	Min. switching capacity	Response times		External connector	Leakage current	Outputs/ common	Fuses (see note)	External power supply capacity	Internal current consumption (5 V DC)	Weight
				ON delay	OFF delay							
CQM1-OD211	8 pts	2 A at 24 V DC $^{+10\%}/_{-15\%}$ 5 A/Unit	---	0.1 ms max.	0.3 ms max.	Terminal block	0.1 mA max.	8	7A (one fuse/ common)	24 V DC $^{+10\%}/_{-15\%}$ 15 mA min.	90 mA max.	200 g max.
CQM1-OD212	16 pts	50 mA at 4.5 V DC to 300 mA at 26.4 V	---	0.1 ms max.	0.4 ms max.		0.1 mA max.	16	5A (one fuse/ common)	5 to 24 V DC ±10% 40 mA min.	170 mA max.	180 g max.
CQM1-OD213	32 pts	16 mA at 4.5 V DC to 100 mA at 26.4 V	---	0.1 ms max.	0.4 ms max.	Connector	0.1 mA max.	32	3.5A (one fuse/ common)	5 to 24 V DC ±10% 110 mA min.	240 mA max.	180 g max.
CQM1-OD214 (PNP, sourcing)	16 pts	50 mA at 4.5 V DC to 300 mA at 26.4 V	---	0.1 ms max.	0.4 ms max.	Terminal block	0.1 mA max.	16	3.5A (two fuses/ common)	5 to 24 V DC ±10% 60 mA min.	170 mA max.	210 g max.
CQM1-OD215 (PNP, sourcing)	8 pts	1.0 A at 24 V DC $^{+10\%}/_{-15\%}$ 4 A/ Unit	---	0.2 ms max.	0.8 ms max.		0.1 mA max.	8	Short-circuit protection function	24 V DC $^{+10\%}/_{-15\%}$ 24 mA min.	110 mA max.	240 g max.
CQM1-OD216 (PNP, sourcing)	32 pts	0.5 A at 24 V DC $^{+10\%}/_{-15\%}$ 5 A/ Unit	---	0.1 ms max.	0.3 ms max.	Connector	0.1 mA max.	32	7A (one fuse/ common)	24 V DC $^{+10\%}/_{-15\%}$ 160 mA min.	240 mA max.	210 g max.

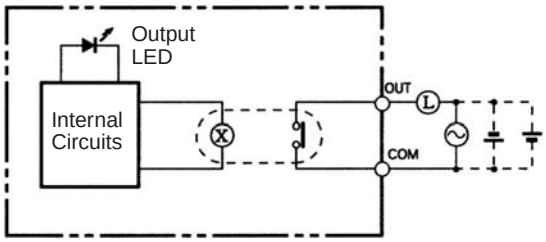
AC Output Units

Model	Number of outputs	Max. switching capacity	Min. switching capacity	Response times		External connector	Leakage current	Outputs/ common	Fuses (see note)	External power supply capacity	Internal current consumption (5 V DC)	Weight
				ON delay	OFF delay							
CQM1-OA221	8 pts	0.4 A at 100 to 240 V AC	---	6 ms max.	1/2 cycle + 5 ms max.	Terminal block	1 mA max. at 100 V AC, 2 mA max. at 200 V AC	4 each (2 circuits)	2A (one fuse/ common)	---	110 mA max.	240 g max.
CQM1-OA222	6 pts	0.4 A at 100 to 240 V AC	100 mA at 10 V AC 50 mA at 24 V AC 10 mA at 100 V AC 10 mA at 240 V AC	1 ms max.	Load frequency of 1/2 cycle + 1 ms max.			4 and 2 (2 circuits)	5A (one fuse/ common)	---	250 mA max.	240 g max.

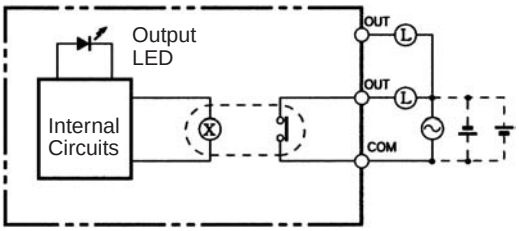
Note: Fuses are not user-serviceable.

■ Circuit Configuration

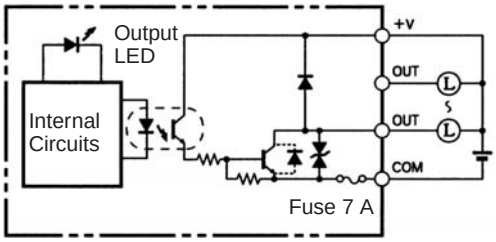
CQM1-OC221



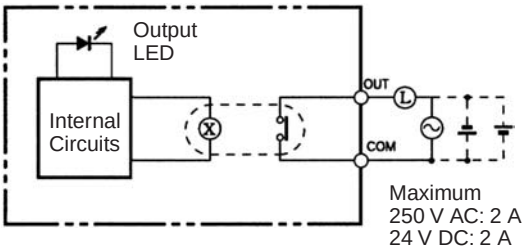
CQM1-OC222



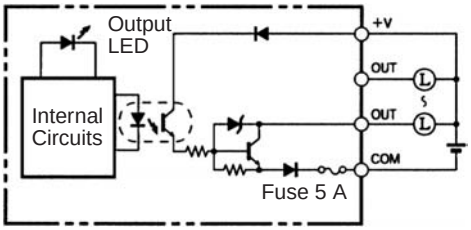
CQM1-OD211



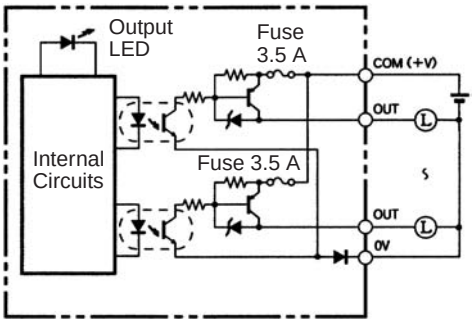
CQM1-OC224



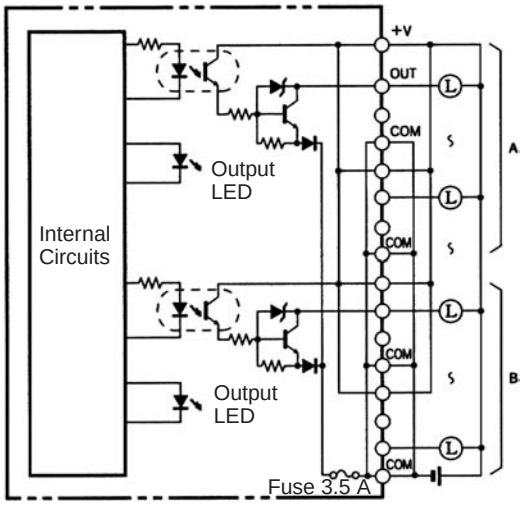
CQM1-OD212



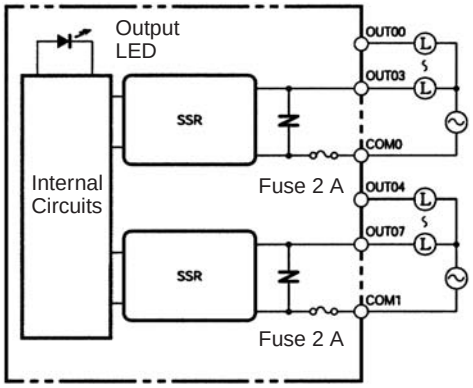
CQM1-OD214



CQM1-OD213

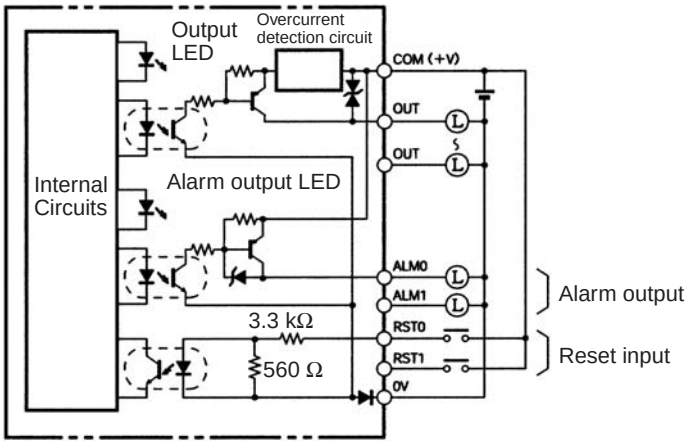


CQM1-OA221

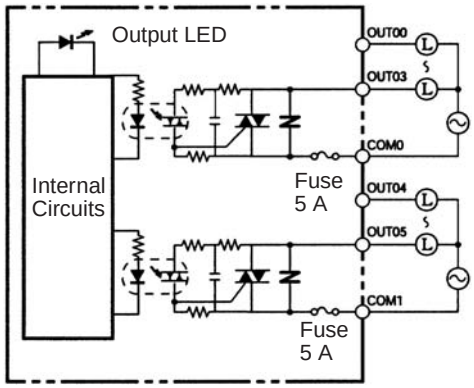


CPU Unit Descriptions

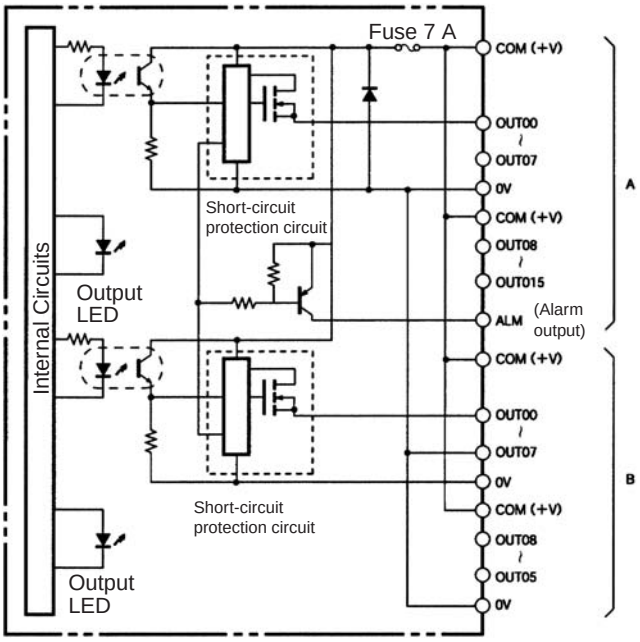
CQM1-OD215



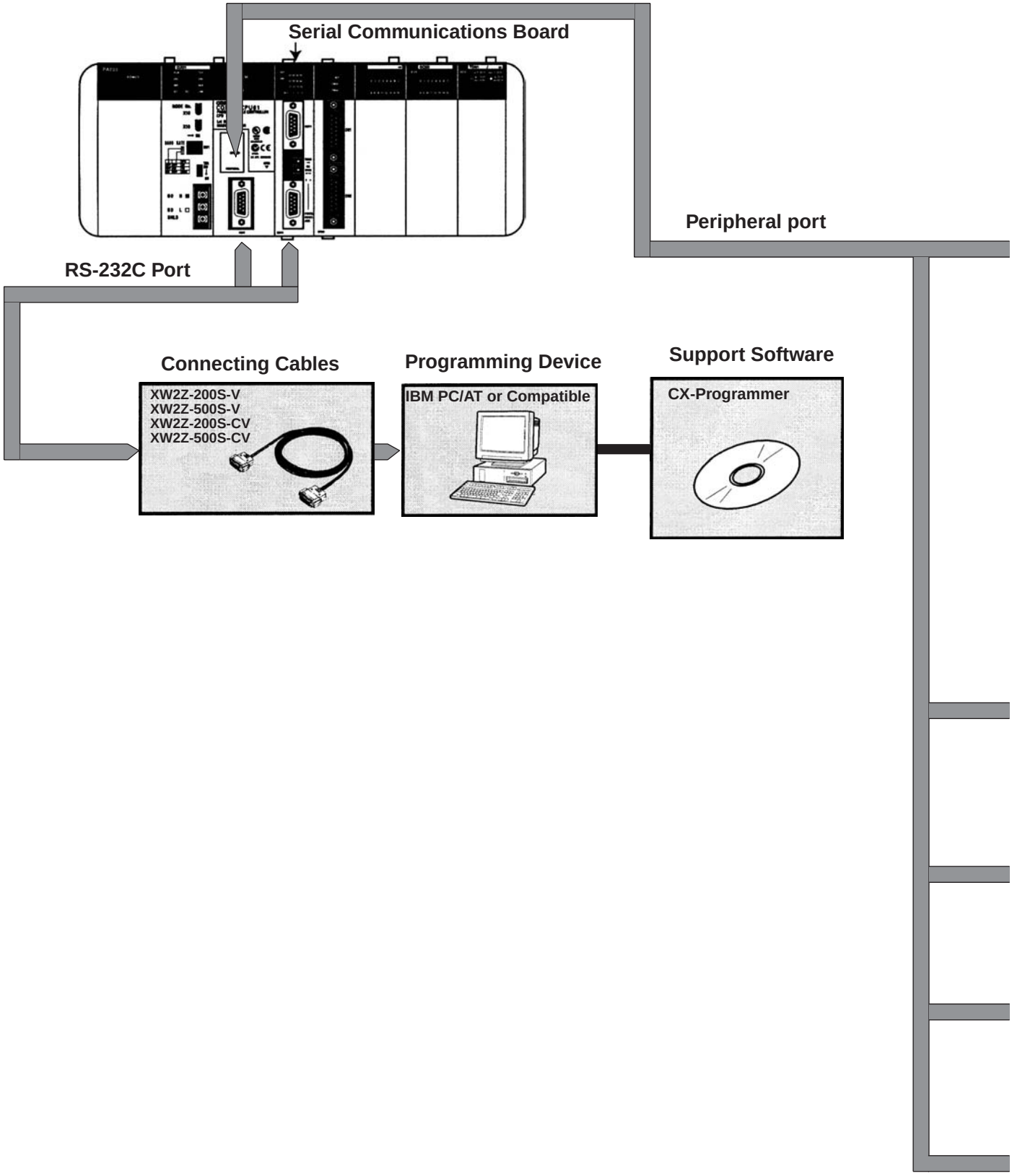
CQM1-OA222

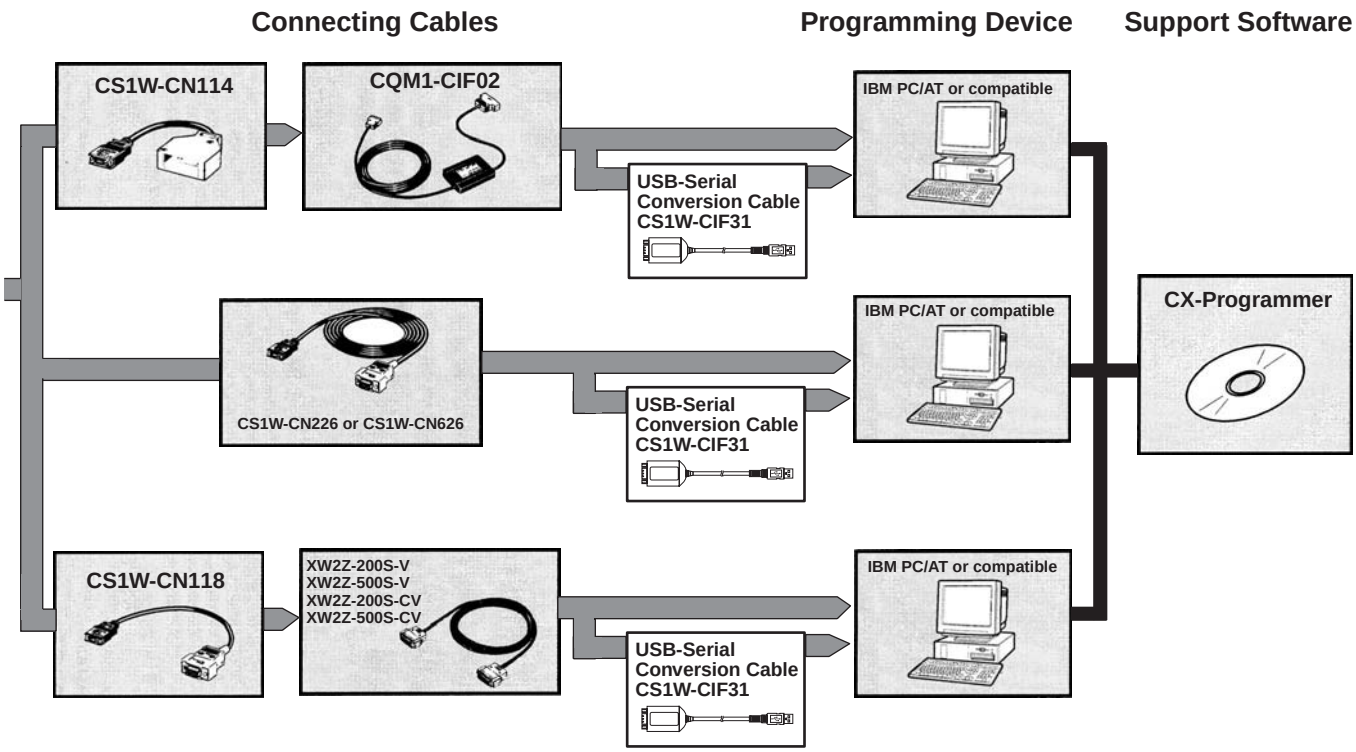


CQM1-OD216

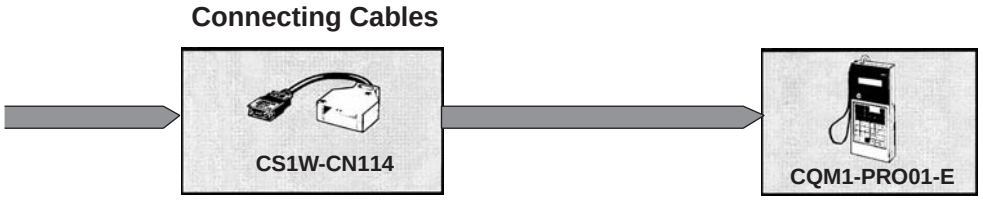


Programming Devices




Connecting Cables
Programming Device
Support Software
CS1W-CN114
CQM1-CIF02
IBM PC/AT or compatible
USB-Serial Conversion Cable CS1W-CIF31
CS1W-CN226 or CS1W-CN626
IBM PC/AT or compatible
USB-Serial Conversion Cable CS1W-CIF31
CX-Programmer
CS1W-CN118
XW2Z-200S-V
XW2Z-500S-V
XW2Z-200S-CV
XW2Z-500S-CV
IBM PC/AT or compatible
USB-Serial Conversion Cable CS1W-CIF31


Programming Console
CQM1H-PRO01-E


Connecting Cables
CS1W-CN114
CQM1-PRO01-E

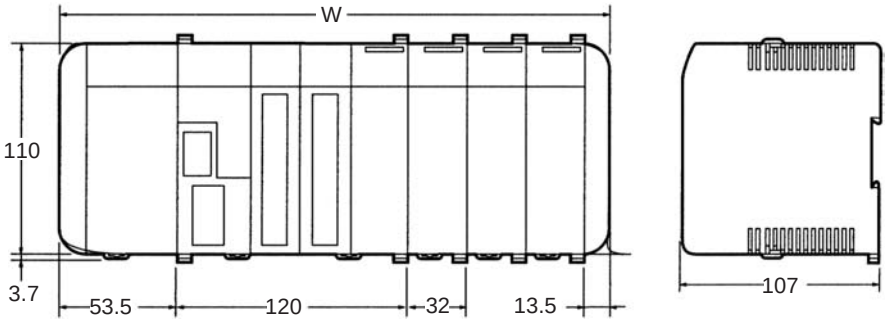

CS1W-CN114
C200H-CN□22
C200H-PRO27-E


CS1W-CN224 or CS1W-CN624
C200H-PRO27-E

Dimensions

Note: All dimensions are in millimeters.

■ Overall CQM1H Dimensions



Overall PLC Widths for Example Configurations

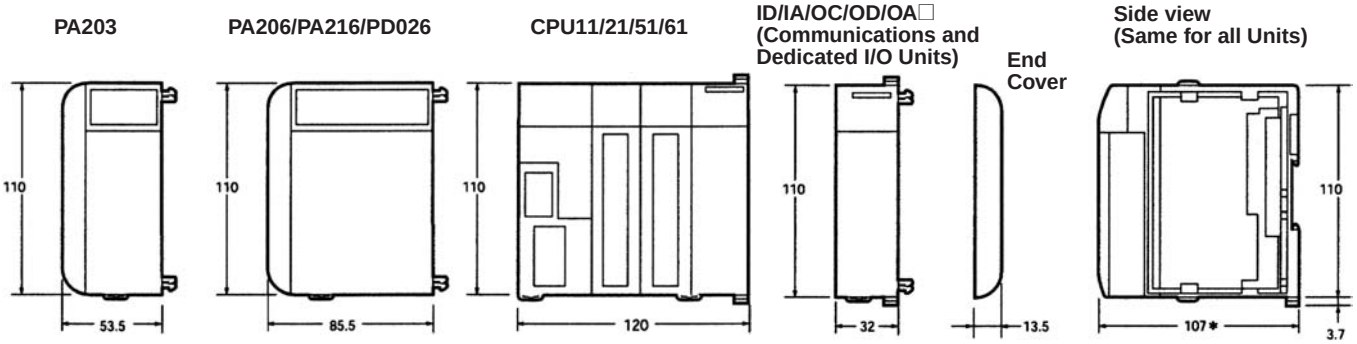
Number of I/O Units	PA203 Power Supply Unit	PA206, PA216, or PD026 Power Supply Unit
	W (mm)	W (mm)
3	283	315
4	315	347
5	347	379

Calculating Overall PLC Width with "n" I/O Units

Power Supply Unit	W (mm)
CQM1-PA203	32 × n + 187
CQM1-PA206	32 × n + 219
CQM1-PA216	
CQM1-PD026	

Note: The total number of I/O Units and Dedicated I/O Units (n) is limited to 12 Units (11 without a Communications Unit) for the CQM1H-CPU51/61 and 11 Units for the CQM1H-CPU11/21.

■ Power Supply, CPU, Communications, Dedicated I/O, and I/O Units



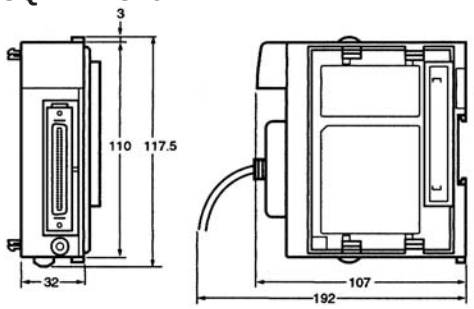
*The CQM1-OC224 is 131.7 mm wide.

Name	Model	Weight
Power Supply Units	CQM1-PA203	460 g max
	CQM1-PA206	560 g max
	CQM1-PD026	
	CQM1-PA216	
CPU Units	CQM1H-CPU11	500 g max.
	CQM1H-CPU21	510 g max.
	CQM1H-CPU51	
	CQM1H-CPU61	
Input Units	CQM1-ID211	180 g max.
	CQM1-ID111	
	CQM1-ID212	
	CQM1-ID112	160 g max.
	CQM1-ID213	
	CQM1-ID214	
	CQM1-IA121	210 g max.
	CQM1-IA221	

Name	Model	Weight
Output Units	CQM1-OC221	200 g max.
	CQM1-OC222	230 g max.
	CQM1-OC224	270 g max.
	CQM1-OD211	200 g max.
	CQM1-OD212	180 g max.
	CQM1-OD213	160 g max.
Output Units	CQM1-OD214	210 g max.
	CQM1-OD215	240 g max.
	CQM1-OD216	210 g max.
	CQM1-OA221	240 g max.
	CQM1-OA222	

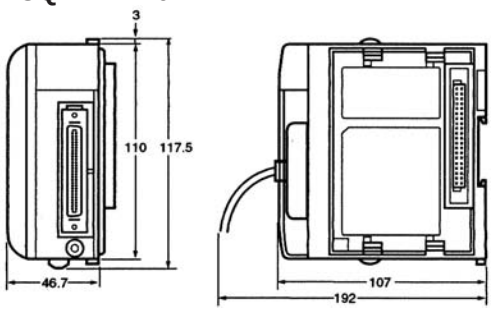
CPU Unit Descriptions

CQM1H-IC101



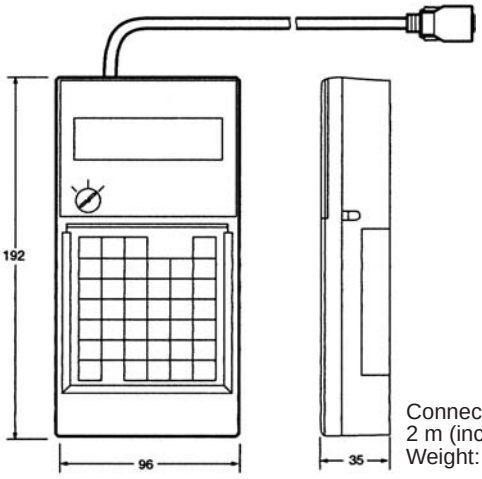
Weight: 131 g max.

CQM1H-II101



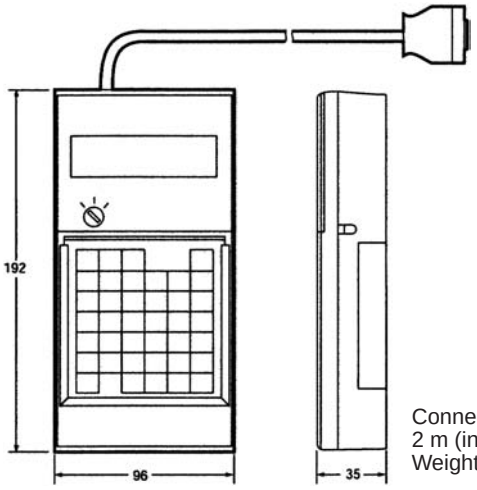
Weight: 211 g max.

Programming Console CQM1H-PRO01-E



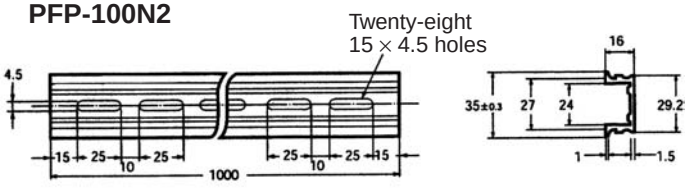
Connecting cable length: 2 m (included)
Weight: 515 g max.

Programming Console CQM1-PRO01-E

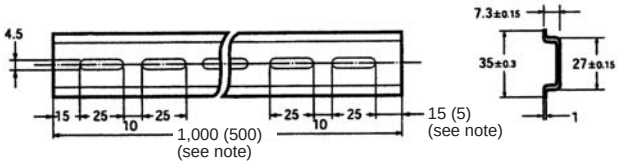


Connecting cable length: 2 m (included)
Weight: 515 g max.

DIN Track PFP-100N2



PFP-100N/50N



Note: The figures in parentheses are for the PFP-50N.